THEORY OF OP MANUAL
FOR THE 256K CPU

Revised for the 256K CPU
by
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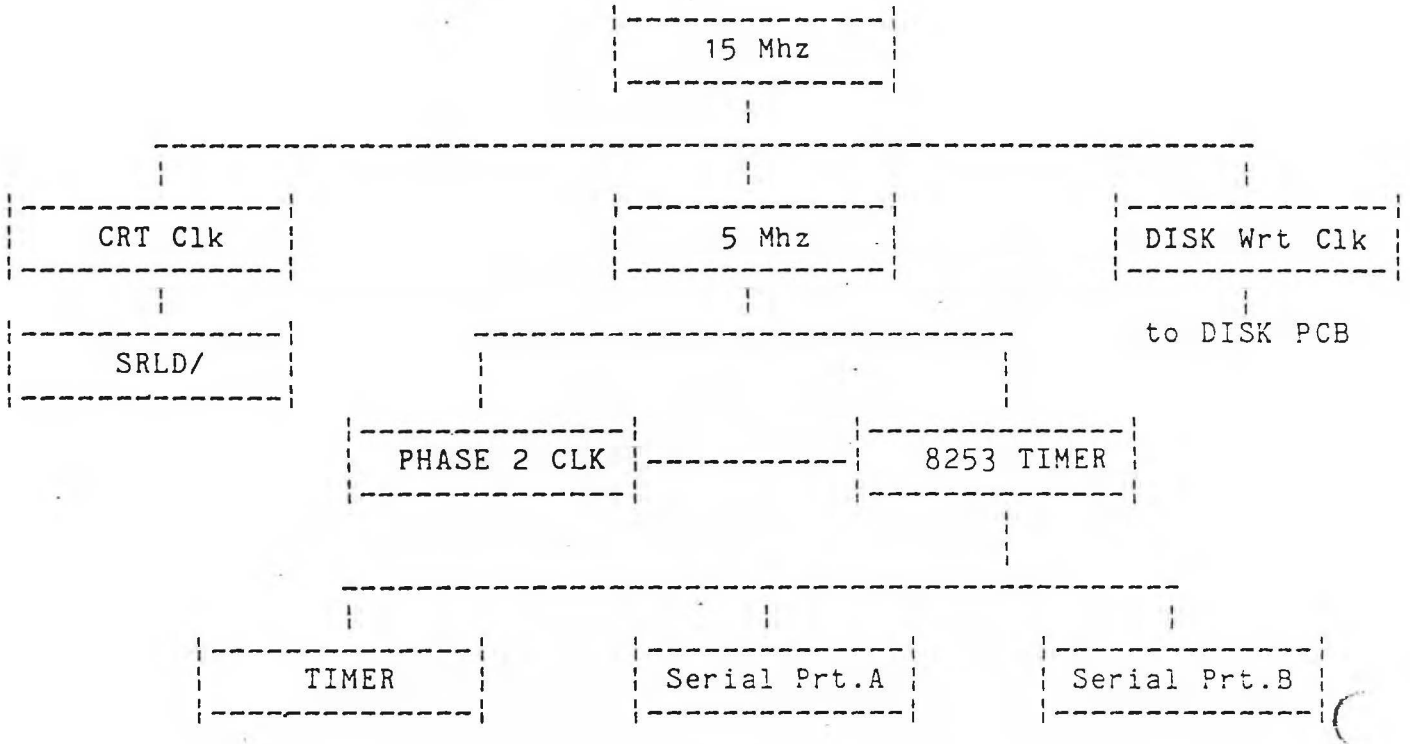
II. CLOCKS

This file discribes the functional operation of the CPU clocks. We will begin with the 15 Mhz clock, which is the driver of the clocks we are to discribe.



A. 15 Mhz Clock -- Refer to CPU schematics 102011 page 4.

The oscilating package at 1J provides a TTL compatible 30Mhz clock with a 50-50 duty cycle at its output pin #8. This package has its own internal biasing and feedback loops and needs no external support circuitry except +5 volts and ground. The 30Mhz clock is buffered by pins 1 and 2 of 1K(74S04). The buffered clock is then routed to the clock input(pin 13) of the JK flip-flop at 7N. Since both the J and K inputs are tied high each falling edge of the 30Mhz clock causes the Q output(pin 9) to toggle dividing the 30Mhz clock by 2 producing a 15Mhz clock with a 50-50 duty cycle. This clock is further buffered by 1K at pins 3, 5, and 13 producing CLK15B, CLK15C, and CLK15A respectively.

B. 5 Mhz Clock -- Refer to page 4.

The 5 Mhz clock is derived from the 15 Mhz clock. Assuming that both flip-flops(f/f) at 2K were initially reset; on the first falling edge of Clk15B the Q output at pin 5 will set high as the inputs were J=1 and K=0.

On the second falling edge of Clk15B, the Q output at pin 9 will

set high and the Q output at pin 5 will toggle low as the inputs were J=1 and K=1.

On the third falling edge of Clk15B, the Q output at pin 9 will reset low(inputs J=0 and K=1) and the Q output at pin 5 will remain idle as the inputs were J=0 and K=0.

The next clock from Clk15B will repeat the above action and our circuit acts as a divide-by 3 network. Clk5 is again buffered, going to the expansion connectors as well as the disk drive PCB.

C. CRT Clock -- Refer to page 8.

The CRT clock is also driven from the 15 Mhz clock but operates at two pre-defined frequencies. In the text mode, device 4P will count from 6 to 15 and act as a divide by 10 counter as the ripple carry output will pre-load a 6. The period of the CRT clock in the text mode is 666ns.

In the high resolution mode(HIRES), device 4P will count from 0 through 15 and acts as a divide by 16 counter as the ripple carry output will pre-load a 0. The period of the CRT clock in the high resolution mode is 1.06 uS.

D. DISK Wrt Clock -- Refer to page 6.

The disk write clock is used on the disk drive PCB for a stable write frequency when writing data to the diskette, and is also used for syncronization of an interrupt to the CPU when the GCR circuitry detects an address mark on the diskette.

The disk write clock is another clock driven by the 15 Mhz clock. Device 13J divides the 15 Mhz by 32. The 74LS393 contains 2 hex counters. The first counter A divides the 15 Mhz clock by by 16 and the second counter B futher divides this output at pin 6 by 2. The end result is a clock with a period of 2.13 uS.

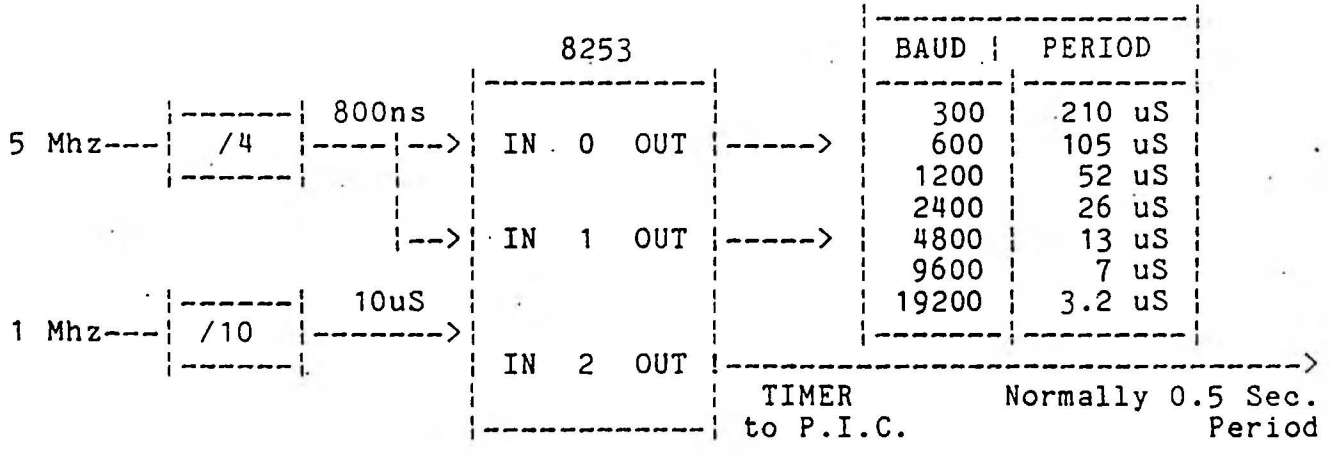
E. PHASE 2 Clock -- Refer to page 5.

The PHASE 2 Clock is driven from the 5 Mhz clock. Device 12E acts as a bi-quinary counter (see truth table). The resulting output is a clock with a period of 1 uS. This output QC (inverted by a 74S04 at 12E), is routed to the disk drive PCB,the expansion connectors, all 65XX devices, and the Phase 2 sync circuitry.

COUNT	QD	QC	QB	
0	L	L	L	
1	L	L	H	<---- start of cycle
2	L	H	L	
3	L	H	H	
4	H	L	L	
5	L	L	L	
6	L	L	H	<---- IOLAT/ here & clear IORDY/
7	L	H	L	<---- end of cycle
8	L	H	H	
9	H	L	L	

F. 8253 PROGRAMABLE TIMER -- Refer to page 14.

The 8253 is a programable timer. It is used to provide the two internal clocks necessary for the serial communications circuitry and also the Timer interrupt going to the P.I.C.



IV. 8088 INTERFACE. Refer to pages 2 and 3.

The 8088 interface consists of the address buffers, data buffers, control buffers/latches, boot PROM'S, and the P.I.C. We will start the discussion with a brief discription of the 8088 basic timing.

The basic machine cycle begins with signal ALE asserted during first uPU clock. During this time that ALE is high; the low order addresses A0-A7 are presented to the AD0 - AD7 lines, and the upper nibble of addresses A16-A19 are presented to the A16/S3 - A19/S6 lines. The second and third uPU clocks will initiate the following events: either RD/,WR/, or INTA/ will go low, lines AD0 - AD7 will drive or recieve data, lines A16/S3 - A19/S6 will reflect internal uPU status, and if the uPU Ready line was low -- the uPU will have entered a wait(s) state(s). The last uPU clock will have the 8088 tri-state the AD0 - AD7 and A16/S3 - A19/S6 lines, and the RD/,WR/ or INTA/ will go back high. Address lines A8-A15 are true during the entire machine cycle.

ADDRESS. Address lines A0-A7 and A16-A19 are de-multiplexed from the AD0 - AD7 and A16/S3 - A19/S6 lines by the 74LS373 transparent latches at 10L and 8P. The gate inputs (pin 11) on these 74LS373's are driven by buffered ALE. The output pins will follow the inputs during the time ALE is high, and the falling edge of ALE will latch the input address and hold this address true until the next ALE. Device 10L is enabled by HLDA (hold ack) and will tri-state when HLDA is high.

Address lines A8-A15 are buffered by a 74LS244 at 8N. This device will pass the input data as long as the enable pins 1 and 19 are held low by buffered HLDA.

DATA. The uPU data lines have separate read, write, and I/O data buffers.

All read operations, excluding PROM'S at 7J & 8J and the P.I.C. at 7L, will be read back thru the 74LS373 at 12L. This device is enabled (pin 1) by the gating of device 11K. If the following conditions are true, device 11K will enable 12L to pass data thru to the uPU: there is no HLDA/ on pin 12 of 11K, there is a read operation condition (gated RD/ "and" DEN/ from device 10K) on pin 1 the P.I.C is not selected by IOD0/ on pin 13, and the PROM'S are not selected by RS1/ on pin 9. The gate input (pin 11) on the 74LS373 at 120K is controlled by the SET/RESET flip-flop action of the circuitry by devices 11D & 14D. Signal ALE/ (12D8) will "SET" device 14D pin 6, signal DLATCH/, high the beginning of each machine cycle. Signals MLAT/ or IOLAT/ (11D pins 4 and 3) will "RESET" device 14D pin 6 low and latch the data present at the inputs of 12L. Signal MLAT/ is asserted at the end of a dynamic ram access generated by the uPU, and signal IOLAT/

is asserted during the end of a Phase2-syncronized IO access.

All write operations, excluding writes to the P.I.C. at 7L, will be buffered thru the 74LS245 at 11L. The enable (pin 19) of device 11L, is controled both signals DT/R (1=write, 0=read) and ALE (forcing the multiplexed addresses A0-A7 onto the buffered bus lines BD0-BD7 during the time ALE is high). The direction input pin 19 (1=A to B, 0=B to A) is controlled by signal HLDA. During a DMA access, when HLDA is high, the 74LS245 at 11L will be passing the data from the buffered BD0-BD7 lines on to the AD0-AD7 lines allowing and external device to control the low order address lines A0-A7 thru the 74LS373 at 10L.

All IO bus transfers will be buffered by the 74LS245 at 13L. The enable (pin 19) of this 74LS245 is driven from the de-coding of the IO devices located on both the CPU and DISK DRIVE P.C.B. Whenever address space E000:0 thru E800:FFFF is asserted "and" an external IO device has not acknowledged to this address (device 13D on page 5), this 74LS245 will be enabled. The direction input (pin 1) is controlled by both signals DT/R and ALE. The inverter at 11M pin 2 will be low whenever DT/R is high for a write operation "or" ALE is high (forcing the addresses A0-A7 onto the ID0-ID7 bus lines). When an IO device is read; the data path is from the ID0-ID7 lines thru the 74LS245 at 13L and unto the BD0-BD7 lines, then latched by IOLAT/ into the 74LS373 at 12L and passed thru to the uPU AD0-AD7 data lines. When an IO device is written to; the data path is from the uPU AD0-AD7 lines thru the 74LS245 at 11L unto the BD0-BD7 lines, then thru the 74LS245 at 13L and unto the ID0-ID7 data lines.

CONTROL. The 8088 control signals are buffered by the 74LS244 at 10M. This buffer will pass the input data as long as there is not a HLDA. When HLDA is asserted by the uPU, the 74LS244 at 10M will be tri-stated to allow an external device to gain control of the bus.

The READY input to the uPU when low will cause the 8088 to enter a wait state (all outputs remain asserted). The 8088 will remain in this wait state until the READY line returns high. One of three sources can pull the ready line low: XACK/ from one of the expansion connectors, IORDY/ selecting one of the IO devices requiring sync with the Phase 2 clock, and PRQ/ requesting a memory access to low 256K dynamic ram or screen ram at FFFF:0. Device 13K pin 6 will go low when one of its three inputs requests a wait state. This clears the 74S112 at 7N and the 8088 READY input is low. When 13K pin 6 returns high, the next falling edge of the uPU clock will set the READY input back high and the 8088 will continue.

The TEST/ input to the uPU is used in conjunctin with the 8088 instruction "WAIT". When the 8088 is issued the "WAIT" instruction, if the TEST/ input is high the uPU will remain idle until the TEST/ input goes low. This input is driven by a signal LBRDY/ (latched-byte-ready) which originates from the DISK DRIVE P.C.B.

This signal is used to detect when a byte of data is ready to read from the GCR circuitry.

The HOLD/ and NMI/ inputs are driven from a device on one of the expansion connectors. These signals are only inverted by device 11M and the timing of these signals must originate from the driving device.

P.I.C. 8259. The 8259 is a priority interrupt controller that signals the 8088 that an IO device needs servicing by setting the INTR signal high. The uPU acknowledges the P.I.C. by asserting INTA/ low. The P.I.C. will then place on the AD0-AD7 bus a vector that the 8088 uses to find an address that will have the IO service routine. The P.I.C. is on the multiplexed AD0-AD7 data lines and is read directly by the 8088 without any data buffering. However the IWR/ and IRD/ signals are buffered by device 12K pins 6 and 8 (page 5). The following table reflects the eight inputs to the 8259.

IRQ	SIGNAL	IO FUNCTION	PAGE
0	SYN	DISK DRIVE ADDRESS SYNC	15
1	COMM	7201 SERIAL COMMUNICATIONS	14
2	TIMER	8253 PROGRAMABLE TIMER	14
3	PARRALLEL	65XX SERIES OF DEVICES	7
4	IR4	EXPANSION CONNECTOR	15
5	IR5	EXPANSION CONNECTOR	15
6	KBINT	6522 KEYBOARD INTERFACE	6
7	VINT	46505 VERTICAL RETRACE	9

PROMS. The PROM'S located at 8J and 7J contain the 8088 boot program that initializes the IO and memory areas and then loads the Operating System (CP/M or MSDOS) into memory. Routines in these PROM'S also check the functionality of various circuits vital to system operation. If error conditions are found, the code instructs the 8088 to enter various "error loops" . The absolute address of these "error loops" will vary with the version of PROM'S being used. There are two different types of devices that the CPU board will accept, 2732 PROM and 2364 ROM. To configure the CPU board for the type device used there is a cut-and-jump trace area. These jumpers route the addresses A11, A12, and A13 to the appropiate logic and socket pins to enable proper device operation. Location 8J contains the PROM marked "FF" and location 7J for PROM "FE" when using 2732'S. When the CPU board is configured for the 2364 ROM, this device is located in the 8J socket.

V. DECODING. Refer to page 5.

The decoding on the CPU board is broken into 4 major boundaries:

ADDRESS	0000:0	DYNAMIC RAM 256K
TO	3FFF:0	
ADDRESS	E000:0	ALL IO DEVICES
TO	E800:FF	
ADDRESS	F000:0	SCREEN RAM 4K
TO	F000:FFF	
ADDRESS	F800:0	PROM/ROM
TO	FFFF:F	

The 74LS138 at 11H will decode memory space at 0000:0. (pin 15), 2000:0(pin 14) and memory space E000:0 and F000:0 (pin 7). When memory space E000:0 and above is selected, the 74LS139 at11J decodes A16 and A15 for selection of PROM/ROM on pin 7, SCREEN RAM on pin 6, 65XX IO on pin 5, and INTEL type IO on pin 4. Selecting memory space E000:0 and E800:0 requires the 8088 to be syncronized with the Phase 2 clock. The NAND gate at 14D pin 3 will go high whenever either of these two memory spaces are selected, and the 74LS112 at 11E pin 3 will latch this on the falling edge of ALE. The Q/ output (pin 6) is signal IORDY/ that will cause the 8088 READY line to be pulled low and put the uPU into a wait state. The JK flip-flop at 11E pins 11, 12, and 9 will clock thru signal CSEN (11E pin 9) on the falling edge of the Phase 2 clock generated by device 12E (refer to discription of Phase 2 clock). Note that the 74LS138 at 12J (65XX decoder) is enabled on the falling edge of the Phase 2 clock with signal CSEN high, and disabled by CSEN low on the next falling edge of the Phase 2 clock. During the last state of the Phase 2 clock, the NAND gate at 11D pin 12 (signal IOLAT/) will reset the flip-flop at 11E pins 2, 3, and 5 and release the 8088 READY input. Signal IOLAT/ going low at the end of the Phase 2 clock; when the 65XX devices have valid data, also latches the IO bus data into 74LS373 at 12L (8088 read buffer). The following devices are enable by the 74LS138 decoder at 12J:

ADDRESS	PIN	IO DEVICE	
E800:0 E800:1	12J15	46505 CRT CONTROLLER	Pg. 9
E000:20 E800:2F	12J14	6522 IEEE/CENTRONICS PORT	Pg. 7
E800:40 E800:4F	12J13	6522 KEYBOARD, BRIGHTNESS/CONTRAST	Pg. 6

E800:60 E800:6F	12J12	6852 SSDA (CODEC) INTERFACE	Pg.17
E800:80 E800:8F	12J11	6522 USER PORT	Pg.16
E800:A0 E800:AF	12J10	6522 DISK MOTOR & STEPPER CONTROL	DISK PC
E800:C0 E800:CF	12J 9	6522 DISK STATUS & CONTROL PORT	DISK PC
E800:E0 E800:EF	12J 7	6522 DISK READ & WRITE DATA PORT	DISK PC

The INTEL type IO devices are selected by the 74LS139 at 11J. Though syncronization is required with the Phase 2 clock, the chip selects are not gated with CSEN as the 65XX chip selects were. However the RD/ and WR/ signals going to these devices are gated with 11E pin 5 (signal IORDY) thru device 12K. The following devices are enabled by the 74LS139 decoder at 11J:

ADDRESS	PIN	IO DEVICE	
E000:0 E000:1	11J12	8259 PRIORITY INTERRUPT CONTROLLER	Pg. 3
E000:20 E000:23	11J11	8253 PROGRAMABLE TIMER	Pg.14
E000:40 E000:43	11J10	7201 SERIAL COMMUNICATIONS DEVICE	Pg.14

VI. SCREEN RAM. Refer to page 9.
DYNAMIC RAM. Refer to pages 10-12.

The ram on the CPU board is a dual port ram, ram that can be accessed by both the 8088 and the CRT controller chip. The 8088 can do both read and write operations to ram while the CRT controller chip can only do read operations to ram. The ram is orginized such that the CRT controller addresses the screen ram (or screen buffer) which contains the address of the characters to be displayed along with the attribute information of the displayed character. This character address together with the row addresses RA0-RA3 from the CRT controller form the address which contains the pattern to be displayed (font cells). It is important to remember that all ram accesses are 16 bits wide, and that the 8088 will read or write only to 8 bits by enabling the appropiate buffer thru A0.

Screen ram consists of the two 6116's at locations 6A and 7A. These rams can be addressed by either the 8088 or CRT controller thru the 74LS157 2-to-1 multiplexers at 9A,10A,and 10B. These multiplexers will pass the 1A-4A inputs to the 1Y-4Y outputs when the select input pin 1 is low, and pass the 1B-4B inputs to the 1Y-4Y outputs when the select pin is high. The 8088 addresses A1-A11 are connected to the multiplexers A inputs and the CRT controller addresses MA0-MA10 are connected to the multiplexers B inputs. The signal EBLCA (enable CRT access) is connected to select input, pin 1, on all three multiplexers. When EBCLA is low, the 8088 addresses will be passed to the screen ram, and when EBCLA is high the CRT controller addresses will be passed the screen ram. The screen ram data lines are connected to 74LS245's for data transfer with the 8088 and also to octal latches at 4A and 3B on page 10 for the latching of the font address. When the 8088 accesses the screen ram, the 74S139 at 10C will be enabled by the signal RS0/ asserted low on pin 1. The signal EBCLA/ is the B input to 74S139, and if no CRT access is in progress, signal EBCLA/ will be high and the 74S139 will be selecting either the Y2 or Y3 output. The A input to the 74S139 is A0; so when A0 is low the 8088 is selecting the buffer for the 6116 at 6A, and A0 is high the 8088 is selecting the buffer for the 6116 at 7A. Note that the enable for these 74LS245's (pin 19) is also gated by signal ALE thru device 9B. This is to ensure that the 74LS245 bus transceivers do not drive the BD0-BD7 bus lines during the time that ALE is asserting the multiplexed address A0-A7 on the BD0-BD7 bus. The direction inputs to the 74LS245 (pin 1) is controlled by the 8088 signal DT/R (1=transmitt, 0=receive). The OE/ output enable pin 20 on the 6116's is also gated with DT/R "and" EBCLA/ on device 5N pins 4, 5, and 6. This gate will go high whenever the 8088 is writing to the 6116's to prevent the 6116's from driving their data lines while the 74LS245'S are enableb to write to the screen ram. The WE/ input pin 21 on the 6116's is gated by the Y2 and Y3 outputs of the decoder at 10D along with the signal RAMWRT/. This will prevent any spurious WE/ pulses and also allow only one 6116 to be written to at a time.

DYNAMIC ram consists of four banks of eight 64K x 1bit rams. The bank of ram in column D is the even bank of the lower 128K (MEM0-MEM7) and the bank in column E is the odd bank of the lower 128K (MEM8-MEM15). Columns F and H are the even and odd banks of the upper 128k. Again, the ram is accessed 16 bits at a time but the 8088 only works with 8 bits by enabling either the 74LS244 at 6B or the 74LS244 at 7B. The ram can be addressed by one of three sources: the 8088 thru the 74S257's at 10H and 10E,the latched CRT font address thru the octal latches at 3B and 4A, or the REFRESH addresses thru the 74LS244 at 2B. The dynamic ram requires 2 kinds of addresses during an access; a row address coincident with RAS/ (Row Address Strobe), and a column address coincident with CAS/ (Column Address Strobe). The 74S257 is a 2-to-1 multiplexer that will pass the data from the 1A-4A inputs to the 1Y-4Y outputs when the select input pin 1 is low. When the select input pin 1 is high, the 74S257 will pass the 1B-4B inputs to the 1Y-4Y outputs The 8088 addresses A1-A8 are connected to the multiplexers 1A-4A inputs and the 8088 addresses A9-A16 are connected to the 1B-4B inputs. During an 8088 access, the 74S257's at 10E and 10H will be enabled by the signal EBCLA (1=CRT access, 0=8088 access) asserted low on their enable input pin 15. The signal MUX will drive the select inputs of the 74S257's low during the start of the access and pass the 8088 addresses A1-A8 onto the ram AB0-AB7 address lines. After RAS/ is asserted low the MUX signal will drive high and pass the 8088 A9-A16 addresses onto the ram AB0-AB7 address, followed by CAS/ going low. When a CRT access is granted, the signal EBCLA will be driven high turning off the 74S157 multiplexers and the 74LS374 at 4A will be enabled by signal CRAS/ going low. The signal RAS/ will be asserte to the ram followed by CRAS/ going high with CCAS/ going low. For a REFRESH it is not required to provide a CAS/, so it is only necessary to provide a Row(Refresh) address. This is accomplished by the 74LS393 hex counter at 3A and the 74LS244 REFRESH buffer at 2B. The REFRESH is granted only when a CRT access is requested (EBCLA) and the display is turned off (during a horizontal re-trace or a vertical retrace). When signal EBCLA goes high, signal REFRESH/ is asserted to pin 1 and 19 of 2B. The refresh address of counter 3A is passed onto the ram AB0-AB7 address bus. This is followed by the signal RAS/ asserted to the ram banks and signal MB/ (same timing as CAS/) will clock a new refresh address, MB/ is gated with REFRESH/ at device 10D pins 10, 9, and 8 to ensure that the refresh addresses are advanced only during refresh cycles.

The dymanic ram data in pins are connected directly to the 8088 BD0-BD7 data lines. The data out pins are buffered from the 8088 BD0-BD7 data lines by the 74LS244 read buffers at 5C and 7C. This allows the WE/ signal to the ram be asserted after CAS/, (CAS/ also functions on the ram to drive the data out pins, avoiding bus contention when writing to the ram and having a late WE/). The dynamic ram data out pins also are routed to the font latches at 6C and 7C on

page 13 to provide the characters to the video drivers during a CRT ram access. When the 8088 reads dynamic ram signals EBLCA, LOWRAM/, and RD/ are gated at 2A pins 3, 4, 5, and 6.(Note:All 3 have to be low at the same time to produce an enable at one of the dynamic ram buffers.) This signal is then gated with A0 at 1B pins 1, 2, and 3 and with inverted A0 at 1B pins 10, 9, and 8. If A0 is high this will produce LROEO/(Latch Ram Output Enable for Odd bank) at pin 3. If A0 is low this will produce LROEE/(Latch Ram Output Enable for Even bank) at pin 8. Selection of the lower or upper 128K banks of dynamic ram is done by the gating of EBLCA/ and A17 by the 74LS51 at 9C pins 2, 3, and 6. This signal is gated by the 74LS00 at 1B pins 12, 13, and 11 and with the 74LS32 at 9B pins 4, 5, and 6. If A17 is low the output of 9C(pin 6) will be high. This forces the output of 9B high enabling the production of RAS0/ and CAS0/(RAS/ and CAS/ for the lower 128K bank) along with the gating of MA(1C pin 2 for RAS0/) and MB and REFRESH/(2C pins 3 and 5 for CAS0/). A17 being low causes REFRESH/(1B pin 13) to be inverted at 1B pin 11. This signal is routed to 1C pin 12 for production of RAS1/ and to 2C pin 1 for production of CAS1/. REFRESH/ is also routed to 2C pin 2. All the inputs of 2C have to be high at the same time in order to produce a low(active) output. Since we now have REFRESH/ and inverted REFRESH/ this inhibits the production of CAS1/(Output Enable) for the upper 128K bank. If A17 goes high the output of 9C will go low when EBLCA/ is high. This will force the output of 1B pin 11 high enabling 2C to produce CAS1/ along with the gating of MB and REFRESH/. The low output of 9C is also present at 9B pin 4 which causes the output(pin 6) to become active(high) only when REFRESH is high. If REFRESH is low the output of 9B will inhibit the production of RAS0/ and CAS0/ at 1C and 2C. Likewise if REFRESH/ is low it inhibits RAS1/ and CAS1/ at 1C and 2C.

When the 8088 is writing to ram the 74LS244 buffers are turned off by signal RD/ going high(inactive) at pin 5 of 2A causing the output(pin 6) to go low which keeps the outputs of 1B pins 3 and 8 from going low(active). This will allow the BD0-BD7 lines to drive data into the ram data inputs(pin 2). The 74S139 at 10C which produces the write enable for dynamic ram will be enabled (pin 15) when the following conditions are meet: DT/R/ is high, LOWRAM/ and EBLCA are low, and MUX and MC are high. The decoding of these signals are done by 74S00 at 1C pins 10, 9, and 8, the 74LS27 at 2A pins 1, 2, 13, and 12, and the 74S10 at 2C pins 9, 10, 11, and 8. Once enabled A0 and A17 qualify which column of ram will receive a write enable. If both are low column 0(column D) receives a write enable. If A0 is high and A17 low column 1(column E) is selected. If A0 is low and A17 is high column 2(column F) is selected. And if both are high then column 3(column H) is selected. Note that the write enable pin for dynamic is pin 3.

VII. MEMORY ARBITRATION. Refer to page 8.

The memory arbitration circuitry provides all the timming requirments necessary to read and write to dynamic ram, as well as allocate memory requests to both the 8088 and the CRT display/REFRESH needs. The heart of the circuitry is the 74S112's at 5L and 5K. These flip-flops produce the timing reflected in the truth table in the lower left hand corner of page 8. The states MA, MB, and MC; are equivilent to the following signals: MA = RAS/, MB = CAS/, and MC = RAMWRT/. Two sources can initiate the timing generator; an 8088 memory request for dynamic or screen ram, or a CRT request for a video display/refresh access.

The timing generator MA, MB, MC is started by a logic 1 into the J input of the 74S112 at 5L. Device 4M pin 12 will only be allowed to go high if pins 1, 13, and 2 are all low. This will occur only when any current activity in the timing generator has finished (pin 13 MA and pin 2 MC are only low together during state 0 of the truth table). 4M pin 1 will go low whenever there is a PRQ (processor request) "or" a EBCLA (enable CRT request thru device 4L pins 6, 5, and 4. If the 8088 is the source of the request; the 74S112 at 4N will have been "SET" by the J input being high (by ALE/ and IO/M (1=IO,0=M) thru device 10K pins 11, 12 and 13) and the K input being low (by selecting either screen ram "or" dynamic ram thru device 5N pins 13, 12, and 11). When 4N pin 9 is "SET", the Q/ output on pin 7 (the PRQ/ signal to the ready circuitry) is low and the 8088 enters a wait state. The 74S112 will be reset when the first MA granted to the 8088 is sensed, via device 5M pins 4 (EBCLA/ - high if no CRT request) "and" MA. The MA output on 5L pin 5 is routed to 5L pin 11 for input to MB, to device 1C pin 2 to generateRAS/,(Page 10) to devic 4K pin 2 to generate signal MUX (one-half cycle after RAS/), to device 4M pin 11 to gate off a CRT request till the end of the current memory cycle, and to device 4L pin 9 to hold off resetting EBCLA low until the end of a CRT memory cycle. Signal MB is output on device 5L pin 9 and is routed to device 5K pin 11 for input to MC, to device 2C pin 3 to generate signal. CAS/,(Page 10) and 5L pin 7 the Q/ output is routed to the REFRESH counter via 10D(Page 10) to generate an incremented REFRESH address after signal RAS/ has gone low. The MC output on 5K pin 9 is routed to device4J pin 2 and gated there with DT/R "and" MUX to generate signal RAMWRT/, to device 4M pin 2 and gated with MA to keep the timing generator from re-triggering, and 5K pin 7 the Q/ output is routed to device 4M pin 3 and gated with EBCLA "and" ram select to generate the timing for signal MLAT/ latching data into the uPU read buffer. The timing of signal MLAT/ from the gating when MC/ low at device 4M pin 3 along with MUX/ being high at 5M pin 13 will generate MLAT/ to go low one-half cycle after the start of the state 4 in the truth table. This will latch the data into the 74LS373 at 12L just before the rising edge of CAS/.

A CRT request is generated by the ripple carry from the CRT clock generator at device 4P pin 15. This ripple carry is latched into device 4K pin 12 via the 74S74 at 5J. The Q output(pin 9) is routed to the J input of the 74S112 at 4N which produces CRQX/(CRT Request) on its Q/ output(pin 6). If there is currently no uPU memory cycle in progress and the timing generator is ready to start another memory cycle (device 4M pins 11, 10, and 9 all low), 4M pin 8 will go high and device 5K pin 5 (EBCLA) will be latched high. EBCLA is routed to device 4L pin 5 where the timing generator is triggered, to device 4J pin 11 which enables signal CRAS/, to device 4J pin 3 and gated with MUX and DISPOFF/ to generate CCAS/, and to device 4N pin 2 to reset the signal CRQX/ back high after the CRT request is granted. The Q/ output on device 5k pin 6 (signal EBCLA/) is routed to device 5M pin 4 so that if a 8088 memory cycle is requested by 4N pin 9, it will remain pending until the current CRT access is finished, inhibits device 4N pin 9 from "reseting" low. The timing of the CRT cycle has the following relationship: CRAS/ will go low at the begining of the memory cycle enabling the CRT Row Address before the fall of RAS/, after RAS/ goes low signal MUX will follow one-half cycle later, MUX going high drives signal CCAS/ low enabling the CRT Column Address and signal CRAS/ returns high, signal CRT LATCH goes low and remains low until one-half cycle into the last state of the timing generator when it returns high and clocks the screen and dynamic ram data into the font address latches at 3B and 4A on page 10 and the character latches at 6C and 7C on page 13. Signal SRLD/ is generated by the 74S74 and 4K pin 9 and inverted by device 4L pins 11, 12, 13 and is used to clock the video data thru the pipeline latches on page 13.

VIII. VIDEO INTERFACE. Refer to page 13.

The video interface consists of a 16 bit parallel-to-serial converter to pass the character display and a series of octal latches to pipeline the character attributes to the appropiate character. A 8-to-1 multiplexer works with the attributes to select the required display and ciruitry to adjust the brightness and contrast compliment the video output.

The characters to be displayed are latched into the 74LS374 latches at 6C and 7C. These latches are clocked by CRT LATCH which is a rising edge signal generated at the end of a CRT memory access. The data latched by these 74LS374's is then loaded into two 74LS166 shift registers and shifted out with the 15Mhz clock. The character attributes are latched into the 74LS374 at 11C and then pipelined thru two more 74LS374 latches to match the attributes to the proper character. Two levels of pipelining are necessary to adjust for the screen ram data latched into the font address latches at 4A and 3B, and the latching of the character cell data at 6C and 7C.

The 74S151 multiplexer at 14C is controlled by the video attributes to select the proper video input for the desired display. The inputs available to the multiplexer are true video, inverted video, logic 1, and logic 0. A lit pixel is equivilent to a logic 1 on the input of the multiplexer. For character attributes such as underline and cursor it is only necessary to select a logic level for the attribute rather than have the character cell provide the information. The output of the 74S151 is an inverted output on pin 6 and this output is syncronized with the 15Mhz clock thru the 74S74 at 16B. The output of the 74S74 pin 9 is buffered by the 74S02 at 16A pins 4 and 10. If a pixel is to be lit, pins 4 and 10 of 16A will go high and allow the emmiter of transistor Q3 to drive current into R30. R30 is the resistor on which the composite video is developed. The strength of the signal can be adjusted by limiting the amount of current available to Q3. This is done thru the contrast circuitry of device 15D and resistors R22, R23, and R24; and controlled by the LOWINT (low intensity) attribute thru the 74S74 at 16B pin 6 and transistor Q2. When the LOWINT attribute is on the Q/ output on 16B pin 6 is low and inverted by the 74S04 at 15D pins 13 and 12. 15D pin 12 will be high and this will allow Q2 to turn on. If any of the inverters at 15D pins 2, 4, and 6 are low, part of the current available to the Q3 transistor will be "robbed" thru transistor Q2 and sunk by the inverter that is low. Full contrast will have all the inverters at 15D pins 2, 4, and 6 all low, and no contrast will have all the inverters outputs high and no current will be "robbed" from the video driver Q3.

The brightnes control works similar to the contrast control thru the current divider of resistors R19, R28, R20, R21. The emmiter of Q1 is approximatly 0.7V (Veb) above ground. The current driving

into the emmiter of Q1 will be "robbed" with each logic low on the brightness controls BRT0-BRT2. Full brightness has all three controls BRT0-BRT2 high and the collector of Q1 will be at around -100 Volts. Brightness all the way down has BRT0-BRT2 all low and the collector of Q1 will be at approximatly -150 Volts.

The last control signals to drive the video circuitry are HORZ/ and VERT/ (the horizontal and vertical drive signals). Both signals originate from the 46505 CRT controller on page 9 and are buffered by the 74LS04 at 13A. The signals are passed thru inductors L2 and L3 out to the video connector J13.

IX. I/O Interface.

The I/O Interface devices are used in an interrupt driven mode and require an operating system be loaded into ram for these devices to function. Some of these devices have multi-functions and all are software driven. Always inspect/suspect cables when questioning the functionality of these circuits.

KEYBOARD INTERFACE. Refer to page 6.

The Keyboard Interface is driven by the 6522 at 16J. When the keyboard sends data to the CPU, the KBDATA line is set to the first serial bit to be sent. This KBDATA line is connected to the CB2 input on the 6522, which is configured to accept serial data. The keyboard then asserts the KBRDY/ line low which is inverted at 15R pin 12 and latched by the 74LS74 at 15P with the Phase 2 (inverted) clock. The Q/ output at 15P pin 8 is the strobe on the CB1 input which clocks in the serial data as well as provide a hardware hand-shake back to the keyboard as signal KBACK/. The hand-shaking on signal KABCK/ is gated by the status of the IRQ pin 21 of this 6522. When the eigth bit is clocked in from the keyboard, the 6522 will generate an interrupt to the 8088 by pulling the IRQ line low.The IRQ will inhibit device 16P pins 10, 9, and 8 from providing the hardware hand-shake of KBACK/. This is necessary during the nineth bit, the STOP BIT, a special hand-shake protocal is accomplished thru the PB1 line on pin 11 of the 6522. The IRQ line is inverted by 15R pin 2 and becomes signal KBINT and enables gate 16P 13, 12, and 11 which passes PB1 as the KBACK/ signal. Signal KBINT is the source to the 8259 P.I.C. to interrupt the 8088 that the keyboard needs servicing.

This 6522 at 16J is the interface for the keyboard but handles several other functions on the CPU board. The brightness and contrast controls are thru PORT B bits 2-7. Parallel Port status is monitored thru DAV (CA1 on pin 40) and SRQ/BUSY (CA2 on pin 39) and the parallel port drivers are controlled by TALK/LISTEN (PB0 on pin 10). The Serial Port is sensed thru PORT A bits 4-7, by Signals RIA, RIB, DSRA, DSRB which are buffered by the 1489 at 17 This 1489 at 17H buffers the +/- 12 Volt RS232 signals to an inverted TTL output suitable to the 6522. The Serial Port is furthur controlled by lines INT/EXTA and INT/EXTB (pins 2 and 3). These lines control whether the internal or external clocks are usec on the Serial Ports A and B.

SERIAL INTERFACE. Refer to page 14.

The Serial Port Interface consists of two identical serial ports driven by a 7201 Serial Communications Device. This 7201 is buffere by 1488 RS-232 drivers and 1489 RS-232 recievers and has multiplexer to select either internal or external transmit and recieve clocks. The internal clocks are programable by the 8253 at 13H (refer to discription of 8253 clocks).

The 7201 clock input pin 1 is a 400ns period clock from the 74LS90

at 14E pin 12 which divides CLK5 by two. The recieve clock for Port A is the output of the 2-to-1 multiplixer at 16C pin 7 which selects either the output of the 8253 Clk.0 at 13H pin 10 or the buffered RXCA from the 1489 at 18E pin 11. Likewise, the transmit clock for Port A is the output of the multiplexer at 17C pin 7 which selects either the 8253 Clk.0 or the TXCA signal buffered by the 1489 at 17B pin 4 and 6. The 7201 outputs for Port A requiring driver buffering from 1488's are: TXDA Transmit Data on 18D pins 2 and 3, RTSA/ Ready To Send on 18D pins 4,5 and 6, DTRA/ Data Terminal Ready on pins 9,10 and 8. The 7201 inputs for Port A requiring reciever buffering from 1489's are: RXDA Recieve Data from 18E pins 1 and 3, CTSA/ Clear To Send from 18E pins 4 and 6, and DCDA/ Data Carrier Detect from 18E pins 13 and 11.

Port B is identicle to Port A in interface. The recieve clock for Port B is the output of 16C pin 9 which selects either 8253 Clk.1 from 13H pin 15 or the signal RXCB from the 1489 at 18C pin 11 The transmit clock for Port B is from the multiplexer at 17C pin 9 which selects either the 8253 Clk.1 or the signal TXCB from the 1489 at 17B pin 8. The 7201 Port B outputs requiring 1488 driver buffering are: TXDB at 18B pins 2 and 3, RTSB/ at 18B pins 4,5,and 6 and DTRB/ at 18B pins 10,9 and 8. The 7201 Port B inputs requiring reciever buffering from 1489's are: RXDA at 18C pins 1 and 3, CTSB/ at 18C pins 4 and 6, and DCDB/ at 18C pins 10 and 8.

Two signals from Port A (RIA and DSRA) and two signals from Port B (RIB and DSRB) are buffered by a 1489 at 17H and monitored thru the 6522 at 16J.

PARALLEL (IEEE/CENTRONICS) INTERFACE. Refer to page 7.

The Parallel Port interface is controlled by the 6522at 16L. This device can be configured to generate interrupts from signals NFRD/RFD and SEL/DAC. Port A is the data and Port B is status and control buffered by the 75160 and 75161 line transcievers at 17L and 17M. The control of the transcievers, signal TE Transmit Enable, direction input is from the 6522 at 16J. This 6522 at 16J also senses signals DAV and SRQ/BUSY for generating interrupts.

The CODEC Volume control is generated from the CB2 output at pin 19. This output is configured to produce a 48uS period clock when used for Volume control. The duty-cycle of the output low determines the Volume and is in increments of 6uS. One half Volume would be a 48uS period clock whose output is high for 24uS, one step up in Volume would have a clock whose output is high for 30uS, ect. Full Volume would have CB2 always low and low Volume would have CB2 always high.

USER PORT INTERFACE. Refer to page 16.

The User Port interface consists of a 6522 at 15L that is connected to a 50 pin stake connector at J5. User software

can configure the Port A and Port B inputs for either input or output functions. The CA1,CA2 and CB1,CB2 are also available for user applications. The CODEC Clock is generated from this 6522 and normally is set to 16KHz. The light pen input is thru the J5 connector and then inverted by the 74LS04 at 13A pins 3 and 4.

CODEC INTERFACE. Refer to page 17.

The CODEC interface consists of a 6852 SSDA(Serial Sync Data Adapte at 13B sending serial data to the 55516/32 Coder/Decoder chip at 1 The AUDIO OUT pin 3 of this 55516/32 is buffered and filtered by a series of LM324 OP Amps, Volume is controlled by the switching action of the 4066 CMOS switch at 1P, and amplified by the LM383 at 5R. When recording data the 55516/32 will be sampling its pin 5 AUDIO IN and sending serial data to the 6852 which is read by the 8088 and stored in memory. The 6852 has internal registers to hold three bytes of data. The 8088 will load the bytes to the 6852 and then monitor the 6852 status register to determine when the 6852 has shifted out the data and is ready for more bytes.

The 55516/32 is biased at 5V by the LM324 at 1R pin 14. The input to pin 12 is 5V from the voltagae divider network of R33, R37, and R38.There will be 6V dropped across R33, a 1V drop across R37, and 5V across R38. The input on 17C pin 10 is 6V and the output pin 8 will provide the 6V D.C. bias that the Audio signal will be injecte onto.

The AUDIO OUT pin 3 of the 55516/32 will have a D.C. level of approximately 3V on which a 2Vpp A.C. audio signal is injected. This 2Vpp signal is capacitively coupled thru C16 to the input pin 3 of 1R. The output pin 1 of 1R will reflect the input 6V D.C. bias with the 2Vpp A.C. audio signal. The circuit at 1R pins 5, 6, and 7 with R34, R35, C12, and C11 act as a low pass filter to pass the low freq audio and filter out the digital high freq noise. The output pin 7 of 1R will also have the 6V D.C. bias with the 2Vpp A.C. audio signal.

The 4066 at 1P controls the volume by either passing the true A.C. audio signal at the inputs 1 and 4, or passing just the 6V D.C. bias at the inputs 8 and 11. The switching is done by the signal CODEC VOL buffered by the 7406 at 1N and enabling the A.C. audio when pins 13 and 5 of 1P are at +12V, or enabling the 6V D.C. bias when pins 6 and 12 are at +12V. The duty cycle of this clock determines the volume and is in 6uS increments with a 48uS period. One half volume would be a 48uS period clock that is high for 24uS, one step up in volume would have a clock that is high for 30uS. The output of the 4066 on pins 2,3,9, and 1 is still the 6V D.C. bias with the 2Vpp A.C. audio signal. This signal is stepped down by the voltage divider resistors R42 and R43 and becomes a 50mVpp A.C. audio signal that is capacitivly coupled thru C17 to pin 1 on LM383 at 5R. The LM383 is a audio amplifier delivers 4 Watts to the built in speaker. The gain of 5R is set by resistors R44 and R45 to approximatly 300. Capicitor C18 in this circuit acts as a filter for any frequency generated by the

CODEC VOL clock. The output of the LM383 is then capacitivly coupled to the speaker thru capacitor C24.

The signal CODEC CLK from the 6522 at 15L is essential for the 6852 SSDA to shift out the data and is the sample frequency used by the 55516/32. This clock is buffered by the 7406 at 1N pins 13 and 12. The SM/DTR pin 5 on the 6852 is used as the control for the ENC/DEC (Record/Play) input pin 10 on the 55516/32 and is buffered by the 7406 at 1N pins 1 and 2.

EXPANSION CONNECTOR. Refer to page 15.

The expansion connector provides the signals and power necessary for implimentation of accessory cards. When debugging the CPU P.C.B. one should always remove any accessory cards to eliminate any external interference to the CPU operation. Care should be taken to inspect the connectors for any foreign particles or bent/shorted pins.

SECTION FOUR...FAULT ISOLATION

SECTION FIVE .... CORRECTIVE MAINTENANCE

SECTION SIX .... PARTS CATALOG & SCHEMATICS

* DENOTES TO BE RELEASED